Amendments to the Claims

Listing of Claims

Claim 1 (currently amended): A method for managing an external memory of a microprocessor to achieve more available capacity, the method comprising:

(a) providing an address translator;

(b) using the address translator to translate a page of the external memory and an address within the page pointed by the microprocessor to a physical address of the external memory, [[each]] a common area of each page pointed to by the microprocessor being mapped to ~~a section~~ one common area of the external memory; and

(c) using the microprocessor to access data stored at the physical address of the external memory.

Claim 2 (cancelled)

Claim 3 (currently amended): The method of claim [[2]] 1 wherein the external memory has a plurality of non-common areas.

Claim 4 (currently amended): The method of claim [[2]] 1 further comprising mapping the page of the external memory and the address of the common area of the page pointed by the microprocessor of the microprocessor to the physical address of the common area of the external memory.

Claim 5 (original): The method of claim 1 wherein the microprocessor processes an

instruction set of 8 bits.

Claim 6 (original): The method of claim 1 wherein the microprocessor is an MCS series microprocessor.

Claim 7 (original): The method of claim 1 wherein the external memory is a flash memory.

Claim 8 (cancelled)

Claim 9 (new): A memory accessing system for achieving more available capacity of a microprocessor, the memory accessing system comprising:

an external memory, comprising a common area; and

an address translator, coupled to the microprocessor and the external memory, for translating a page of the external memory and an address within the page pointed to by the microprocessor into a physical address of the external memory, wherein a common area of each page pointed to by the microprocessor is mapped to the common area of the external memory.

Claim 10 (new): The memory accessing system of claim 9 wherein the external memory has a plurality of non-common areas.

Claim 11 (new): The memory accessing system of claim 9 wherein the address translator further maps the page of the external memory and the address of the common area of the page pointed to by the microprocessor to the physical address of the common area of the external memory.

Claim 12 (new): The memory accessing system of claim 9 wherein the microprocessor

processes an instruction set at least 8 bits.

Claim 13 (new): The memory accessing system of claim 9 wherein the microprocessor is an MCS series microprocessor.

Claim 14 (new): The memory accessing system of claim 9 wherein the external memory is a flash memory.